REMARKS

The last Office Action in the above-identified application and the references cited by the Examiner have been carefully considered. The drawings have been amended, in accordance with the Examiner's requirement, and applicants respectfully submit the following comments in support of the patentability of the claims.

In Paragraph 2 on Page 2 of the Office Action, the Examiner contends that Figure 3A should be designated by a legend, such as "Prior Art", and refers to MPEP Section 608.02(g). The Examiner requires corrected drawings in compliance with 37 C.F.R. 1.121(d) in reply to the Office Action to avoid abandonment of the application.

In accordance with the Examiner's request, and to comply with 37 C.F.R. 1.121(d), an annotated sheet, showing Figure 3A, with the term 'Prior Art" shown in red, is submitted herewith for the Examiner's approval. Also, a replacement sheet with the term "Prior Art" added in the page header, as per 37 C.F.R. 1.21(d), is also submitted herewith.

It is respectfully requested that the Examiner approve the changes to Figure 3A, and enter the replacement sheet submitted herewith. However, if the Examiner has any comments or suggestions, or requires further changes to Figure 3A, it is respectfully requested that he contact the undersigned attorney at the telephone number given below.

Claims 1-4, 6-9, 13-16 and 19-23 have been rejected under 35 U.S.C. 102(b) as being anticipated by, or in the alternative, under 35 U.S.C. 103(a) as being obvious over, U.S. Patent No. 6,088,262 (Nasu). Also, Claims 2, 4 5, 10, 11, 17 and 18 have been rejected under 35 U.S.C. 103(a) as being unpatentable over the Nasu patent in view of the prior art disclosed in the subject application. Furthermore, Claim 12 has been rejected under 35 U.S.C. 103(a) as being unpatentable over the Nasu patent in view of the prior art disclosed in the subject application, and in further view of U.S. Patent No. 4,796,258 (Boyce). Although the grounds for the rejection of independent Claim 24 are not stated in the Office Action, it is believed

that the claim has been rejected under 35 U.S.C. 103(a) in view of the combination of the Nasu patent and the prior art disclosed in the subject application.

With respect to main Claims 1 and 13, the Examiner contends that the Nasu patent discloses a method for obstructing access to a secure area of a semiconductor device by providing a control signal indicating that the semiconductor device has entered a secure mode, and refers to Column 9, Line 20 and Column 2, Lines 51-55, and Figures 12A and 15A of the Nasu patent for disclosing this feature. In further regard to this feature, the Examiner contends that the control signal set forth in Claims 1 and 13 of the pending application is equivalent to the read protection signal disclosed in the Nasu patent. The Examiner also contends that the feature of obstructing access to the secure area utilizing the control signal is disclosed in the Nasu patent at Column 9, Lines 12-15.

The Examiner also addressed, individually, the claims which depend from main Claims 1 and 13, and his comments are found on Pages 3-11 of the Office Action.

Also, the Examiner's comments with respect to the combination of the Nasu patent with either the admitted prior art alone or the combination of the admitted prior art and the Boyce patent are found on Pages 7 through 11 of the Office Action.

The rejection of Claims 1-24 in view of the Nasu patent, the prior art disclosed in the subject application and the Boyce patent, alone or in combination, is respectfully traversed. The invention disclosed in the subject application prevents access to a secure area of a semiconductor device when the semiconductor device is in a secure mode. The invention as defined by the claims is also particularly relevant when an in-circuit emulator (ICE) is used and connected with the semiconductor device. None of the references of record discloses the combination of the steps of the methodology and features of the system of the present invention and either an in-circuit emulator or a semiconductor device that enters a secure mode.

In particular, independent method Claim 1 and independent system Claim 13 provide steps and structure, respectively, which prevent access to a secure area of a semiconductor device when the semiconductor device is in a secure mode. The Nasu patent does not disclose the semiconductor device being in a secure mode. As described in the subject application, the semiconductor device is in a user mode or in a secure mode (i.e., supervisor mode), especially when using an in-circuit emulator, and the invention is directed to preventing access to secure areas by a user when the semiconductor device has entered a secure mode. Without such methodology and system as envisioned by the applicants and as set forth in Claims 1 and 13, the purpose of having a secure area is defeated, especially when a user is using an in-circuit emulator. The control signal which is generated indicates that the semiconductor device has entered a secure mode, and obstructs access to the secure area.

The Nasu patent does not disclose a semiconductor device which enters the secure mode, nor does it address the problems inherent with use of in-circuit emulators. The passages referred to by the Examiner in the Nasu patent have been carefully considered, especially Figure 12A and Column 2, Lines 51-57, Figure 15A and Column 2, Lines 24-27, Column 9, Lines 12-15, and Column 9, Lines 16-22, and Figure 10A, and other passages. It is not believed that there is any disclosure in the Nasu patent about the semiconductor device entering a "secure mode". As such, it is respectfully urged that independent method Claim 1 and independent system Claim 13 patentably distinguish over the Nasu patent and are allowable.

The Boyce patent has also been reviewed for the combination of steps and elements set forth respectively in independent method Claim 1 and independent system Claim 13. Again, it is respectfully urged that the Boyce patent does not disclose the features set forth in these claims. As such, it is respectfully urged that Claims 1 and 13 patentably distinguish over the Boyce patent and are allowable.

Independent Claim 24 calls specifically for the connection of an in-circuit emulator, as well as the particular structural features of the system for obstructing access to a secure area of a semiconductor device. Although the Nasu patent discloses a read protection control

circuit 107, and a series of AND gates 801-803, the Nasu patent does not teach or suggest the use of such a circuit when the semiconductor device is connected to an in-circuit emulator, and the problems which are inherent with such use of an in-circuit emulator and how these problems are solved by applicants' system defined by Claim 24. The Boyce patent also does not disclose the combination of elements of applicants' systems set forth in Claim 24, or the use of an in-circuit emulator and the problems inherent with such use of an in-circuit emulator.

None of the references of record, including applicants' prior art disclosed in the subject application, taken alone or in combination, discloses the particular features set forth in Claim 24, or for that matter, Claims 1 and 13. As such, it is respectfully urged that independent Claim 24 patentably distinguishes over the references of record and is allowable.

Claims 2-12 and 14-23 depend directly or indirectly from either Claim 1 or Claim 13. As such, it is respectfully urged that dependent Claims 2-12 and 14-23 patentably distinguish over the references of record for the same reasons submitted with respect to independent Claim 1 and independent Claim 13.

Also, a number of these claims define patentable subject matter in their own right and are, therefore, allowable. For example, Claim 3 particularly calls for the step of selecting a multiplexer channel with the control signal. The Nasu patent, applicants' prior art disclosed in the subject application and the Boyce patent do not disclose that a control signal will select a multiplexer channel for obstructing access to the secure area when the semiconductor device has entered a secure mode. The multiplexer circuit is shown in Figure 6A of the subject application, and its operation is illustrated by Figure 6B. The operation of the multiplexer is further described on Page 8, Line 15 through Page 9, Line 23 of the subject application. It is stated that a state machine may be connected to input 92 of the multiplexer to produce a particular pattern of one's and zero's after the control signal 69 transitions to a logic low (or a logic high) state. The pattern may be, for example, all one's or all zero's, alternating one's and zero's, or any other pattern desired by the semiconductor device developer. No such disclosure is found in the Nasu patent, the Boyce patent or in the prior art

disclosed in the subject application. As such, it is respectfully urged that Claim 3 patentably distinguishes over the references of record, not only for the reasons submitted with respect to Claim 1, but also because the prior art does not disclose the step of selecting a multiplexer channel with the control signal in order to obstruct access to the secure area of the semiconductor device that has entered a secure mode.

Similarly, Claim 5 defines the method of Claim 1, wherein the secure area is used in connection with data encryption. The Boyce patent does not disclose this, nor does the Nasu patent disclose encryption. The prior art disclosed in the subject application merely refers to encryption, but the combination of steps in applicants' method for obstructing access to a secure area of a semiconductor device by providing a control signal indicating that the semiconductor device has entered a secure mode, and obstructing access to the secure area utilizing the control signal, where the secure area is used in connection with data encryption, is not found in any of the references of record or in the prior art disclosed in the subject application. Accordingly, Claim 5, not only because of its dependency on Claim 1 and the reasons submitted with respect thereto, but also because it defines the method of preventing access to the secure area used in connection with data encryption, patentably distinguishes over the references of record and is allowable.

Also, dependent Claim 6 more specifically defines the method of Claim 1 as providing a control signal that further comprises decoding a plurality of signals to generate the control signal. No such feature is set forth in the Nasu patent or the Boyce patent, nor is it disclosed in the prior art set forth in applicants' subject application. In this regard, the Examiner refers to Column 2, Lines 51-57 of the Nasu patent, but there, it only discloses that "[t]he read protection means may have a plurality of the second non-volatile memories; and the read protection means can protect data in the first non-volatile memory from being read out from the outside when at least one of signals output from the second non-volatile memories indicates that the read protection for the first non-volatile memory is enabled." Nowhere in this passage is decoding a plurality of signals to generate the control signal disclosed. Accordingly, it is respectfully urged that Claim 6, not only because of its

dependency on Claim 1, but also because it defines decoding a plurality of signals to generate the control signal, patentably distinguishes over the references of record and is allowable.

Claim 10, which also depends from Claim 1, further defines the method of Claim 1 as including the step of connecting an in-circuit emulator to the semiconductor device. Again, the references of record, in particular, the Nasu patent and the Boyce patent, do not teach or suggest the use of an in-circuit emulator in conjunction with a semiconductor device and a control signal which indicates that the semiconductor device has entered a secure mode, and obstructing access to the secure area utilizing the control signal, as defined by method Claim 10, due to its dependency on Claim 1. An in-circuit emulator is not disclosed in the Nasu patent, nor is there any disclosure of the combination of steps set forth in Claim 10 found in any of the other references of record. As such, it is respectfully urged that Claim 10 patentably distinguishes over the references of record because of its dependency on Claim 1 and also because of the fact that it specifically defines the method of Claim 1 as further including the step of connecting an in-circuit emulator to the semiconductor device.

Claim 11 is dependent on Claim 10 and includes all of the limitations found in Claim 10 and Claim 1, discussed previously. Again, an in-circuit emulator is defined by Claim 11, and specifically, the semiconductor device is defined as entering the secure mode when the in-circuit emulator is connected to the semiconductor device. Again, none of the references of record discloses the particular steps found in Claim 11, directly, or indirectly through its dependency on Claim 10 and Claim 1. As such, it is respectfully urged that Claim 11 patentably distinguishes over the references of record for the reasons submitted with respect to Claims 1 and 10, but also because of the particular steps defined in Claim 11 of wherein the semiconductor device enters the secure mode when the in-circuit emulator is connected to the semiconductor device.

Claim 12 also depends from Claim 10 and incorporates all of the limitations of Claim 10 and Claim 1. The claim further defines the command which is generated by the in-circuit emulator as being a software interrupt. Again, none of the references of record, including the Nasu patent and the Boyce patent, and also the prior art disclosed in the subject application,

discloses that the command is a software interrupt or, for that matter, teaches or suggests the particular steps found in Claim 12, 10 and 1 from which Claim 12 depends. As such, it is respectfully urged that Claim 12 patentably distinguishes over the references of record and is allowable, not only because of its dependency on Claims 10 and 1 and the reasons submitted with respect to the patentability of these claims, but also because it discloses that the command generated by the in-circuit emulator is a software interrupt, and such is not disclosed in any of the references of record.

The dependent system claims similarly define features which are not found in the references of record. For example, Claim 16, which depends from Claim 13, specifically defines the second circuit as being a multiplexer. Again, as stated previously with respect to Claim 3, none of the references of record, including the Nasu patent in particular, or the Boyce patent, or the prior art disclosed in the subject application, discloses that a multiplexer is used as part of the system for obstructing access to the secure area connected to the control signal. Such a multiplexer is not found in any of the references of record. As such, Claim 16 patentably distinguishes over the references of record for the same reasons submitted with respect to Claim 13, but also because it defines specifically that the second circuit is a multiplexer, and such is not found in any of the references of record. As such, it is submitted that Claim 16 is patentable over the references of record and is allowable.

Claim 17 is a dependent claim and depends from Claim 13, and specifically defines the system as including a port for an in-circuit emulator. As stated previously with respect to Claim 24, Claim 10, and Claim 11, the Nasu patent, the Boyce patent and the prior art disclosed in the subject application do not disclose the connection of an in-circuit emulator to a semiconductor device in combination with a circuit which generates a control signal that is utilized to obstruct access to the secure area of the semiconductor device when a mode indicated by the control signal is a secure mode. As such, it is respectfully urged that Claim 17 patentably distinguishes over the references of record because of its dependency on Claim 13 and the reasons submitted with respect thereto, but also because it further defines the system of Claim 13 as including a port for an in-circuit emulator, and is allowable.

Claim 18 depends from Claim 17 which depends from Claim 13 and, therefore, incorporates all of the limitations of Claim 13 and Claim 17. Claim 18 also defines the semiconductor device as entering the secure mode when the in-circuit emulator is connected to the port. For the same reasons submitted with method Claim 11, it is respectfully urged that Claim 18, in its own right, patentably distinguishes over the references of record. None of the references of record, including the Nasu patent, the Boyce patent, or the prior art disclosed in the subject application, teaches or suggests a combination of these features of applicants' system defined by Claim 18, including that the semiconductor device enters the secure mode when the in-circuit emulator is connected to the port. As such, it is respectfully urged that Claim 18 patentably distinguishes over the references of record due to its dependency on Claim 17 and indirectly on Claim 13 and the reasons submitted with respect to the patentability of Claims 13 and 17, but also because none of the references of record specifically disclose the features set forth in Claim 18, and is allowable.

Claim 20 depends from Claim 13, and specifically defines the semiconductor device as an application specific integrated circuit. The Examiner refers to Figure 16 of the Nasu patent for showing this. However, it is respectfully urged that Figure 16 does not specifically show that the semiconductor device is an application specific integrated circuit, and it is believed that nowhere in the Nasu patent is there a disclosure that the semiconductor device is formed as an application specific integrated circuit. It is also believed that none of the other references cited by the Examiner discloses this feature. As such, Claim 20 patentably distinguishes over the references of record because of its dependency on Claim 13 and the reasons submitted with respect to the patentability of that claim, but also because it defines the semiconductor device as an application specific integrated circuit, and is allowable.

Claim 21 depends from Claim 20 and incorporates all of the limitations of Claim 20 and Claim 13 from which Claim 20 depends. Claim 20 specifically defines the system of Claim 21 as having the first circuit as a microprocessor core. The Examiner contends that the Nasu patent discloses a first circuit as a microprocessor core, and refers to Column 2, Lines 51-57 of the Nasu patent for teaching this. However, a reading of the passage referred to in the Nasu patent merely refers to the read protection means as having a plurality of second

non-volatile memories, and further refers to a first non-volatile memory, and that is all. It does not mention the word "microprocessor" in this passage. None of the other references of record, including the Boyce patent or the prior art disclosed in the subject application, teaches or suggests the combination of features set forth in Claim 21. Accordingly, it is respectfully urged that Claim 21 patentably distinguishes over the references of record for the same reasons submitted with respect to Claim 13, but also because the references of record do not disclose the first circuit as being a microprocessor core, and is allowable.

Claim 22 depends from Claim 13, and further defines the first circuit as being a decoder. The Examiner contends that the Nasu patent teaches a first circuit as being a decoder, and refers to Column 2, Lines 51-57 for disclosing this feature. However, a careful reading of Column 2, Lines 51-57 of the Nasu patent does not reveal the disclosure of a decoder as defined by Claim 22. In particular, Column 2, Lines 51-57 of the Nasu patent only refers to the read protection means as having a plurality of second non-volatile memories, and the read protection means can protect data in the first non-volatile memory from being read out from the outside when at least one of signals output from the second non-volatile memories indicates that the read protection for the first non-volatile memory is enabled. Only memories are disclosed, not a decoder. None of the other references of record, including the Boyce patent and the prior art disclosed in the subject application, teaches or suggests the particular combination of elements set forth in the system defined by Claim 22 of the subject application. Accordingly, it is respectfully urged that Claim 22 patentably distinguishes over the references of record for the reasons submitted with respect to Claim 13, but also because none of the references of record discloses a first circuit of the system being a decoder, and is allowable.

Accordingly, it is respectfully urged that Claims 1-24 patentably distinguish over the references of record and are allowable.

In view of the foregoing amendments to the drawings and remarks concerning the pending claims, reconsideration of Claims 1-24 and allowance of the application with Claims 1-24 are respectfully solicited.

Respectfully submitted,

Gerald T. Bodner

Gerald T. Bodner
Attorney for Applicants
Registration No. 30,449

BODNER & O'ROURKE, LLP
425 Broadhollow Road, Suite 108
Melville, NY 11747
Telephone: (631) 249-7500
Facsimile: (631) 249-4508

AMENDMENTS TO THE DRAWINGS:

Figure 3A has been amended to add the legend "Prior Art". A replacement sheet, properly labeled in accordance with 37 C.F.R. 1.121(d), is attached hereto. Also, an annotated sheet, with the requested change marked in red, is also attached herewith. Entry of the changes to Figure 3A is respectfully solicited.

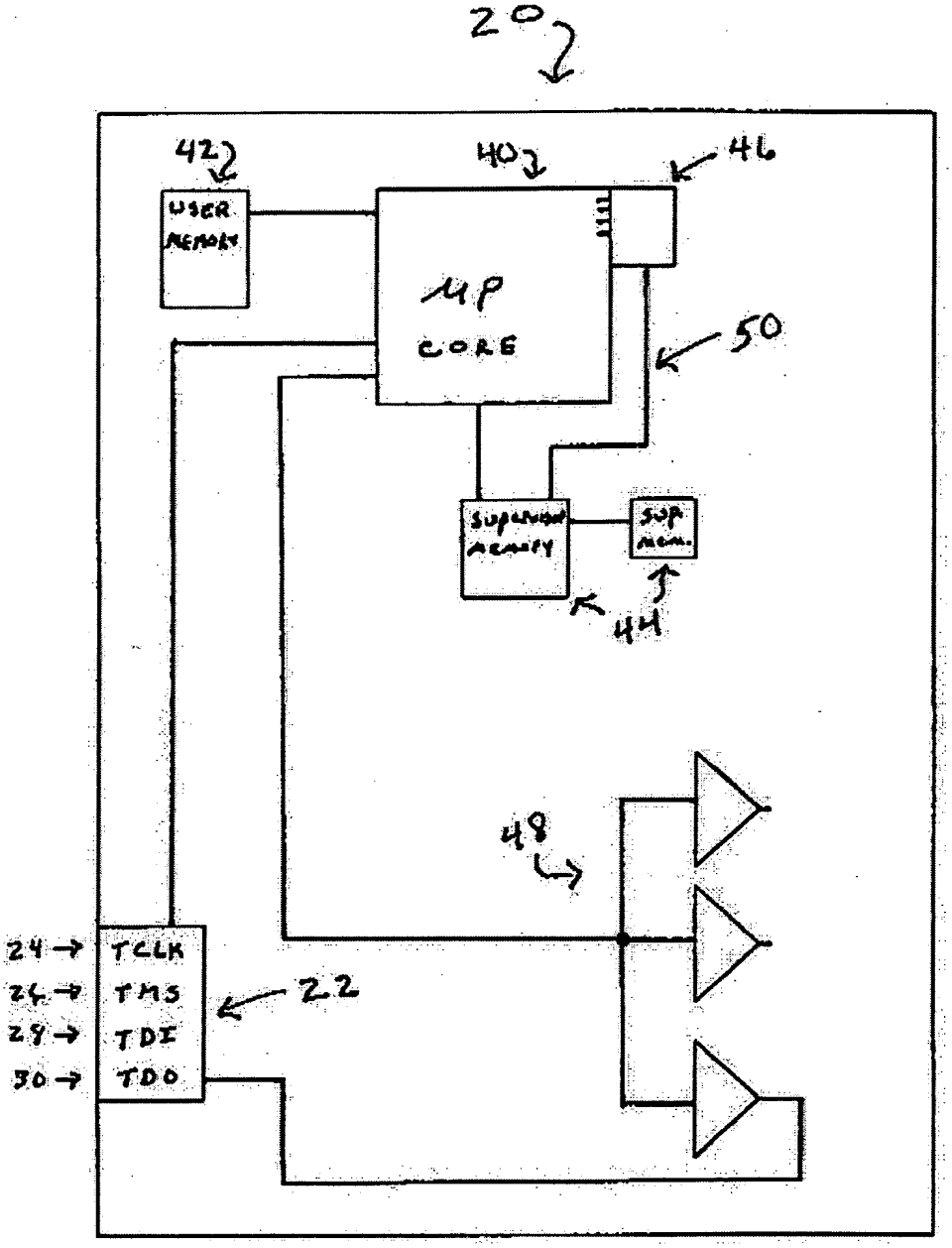

FIG. 3A
PRIOR ART

added